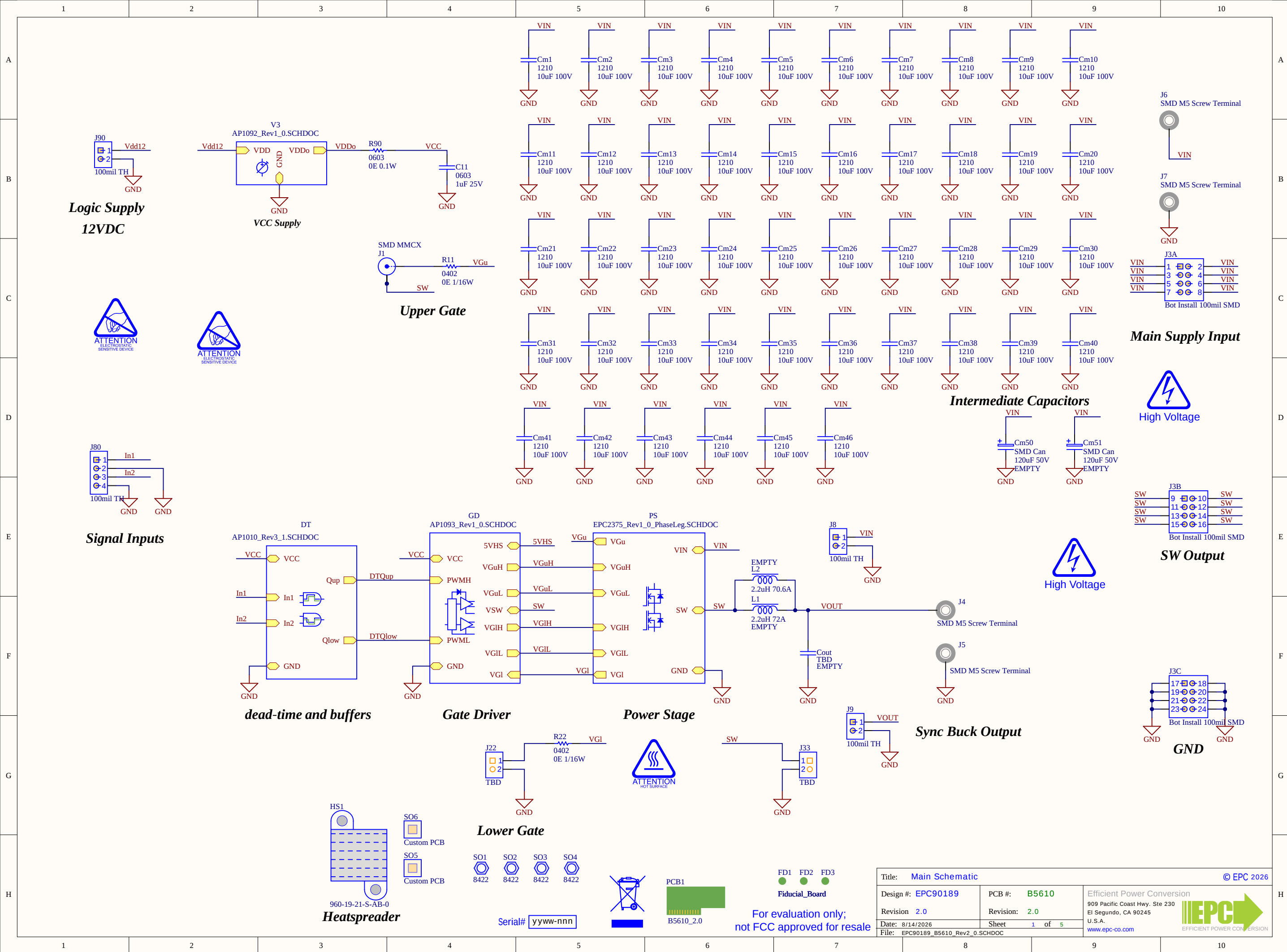
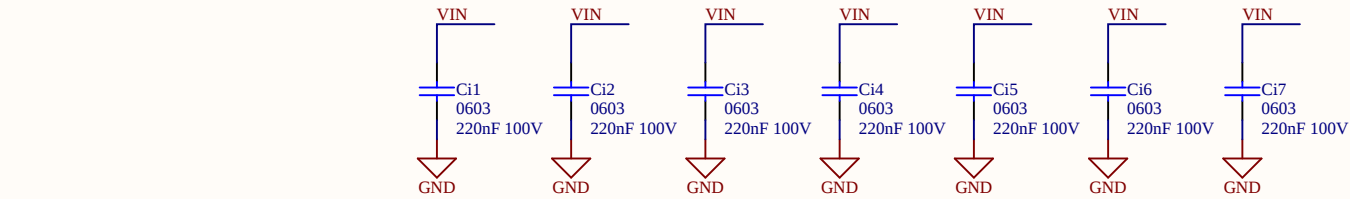




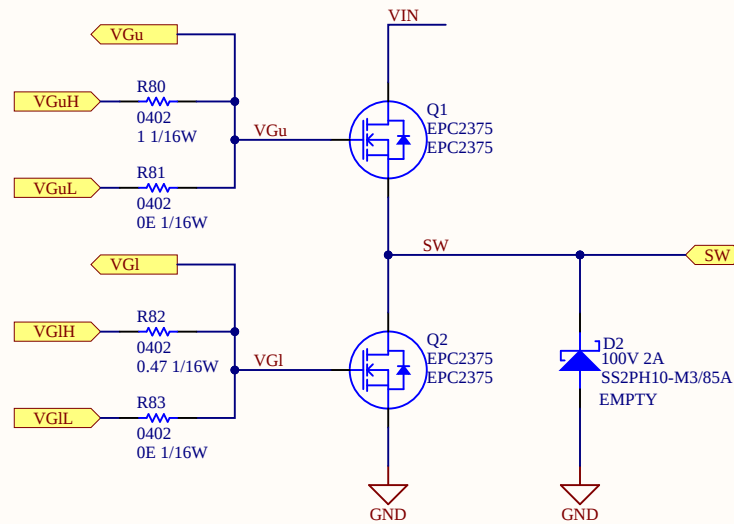
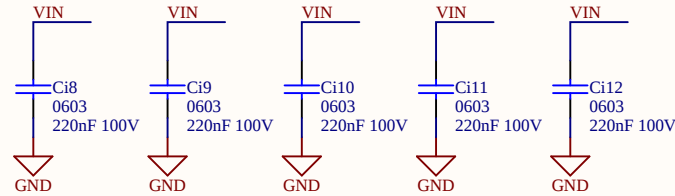


HF loop Capacitors

Vin VIN

GND
GND

**DC Input
40 Vmax.**



Power Stage

Optional Diodes

Title: **HB Sub Schematic - Phase Leg**

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Design #: **EPC2375 Phase Leg**

Revision **1.0** P/N#: **EPC2375**

Date: 8/14/2026

Sheet **2** of **5**

File: EPC2375_Rev1_0_PhaseLeg.SCHDOC

Efficient Power Conversion

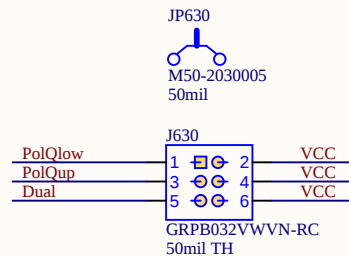
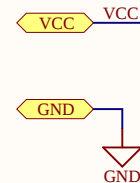
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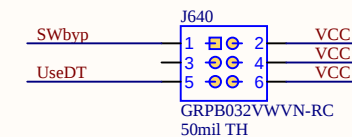
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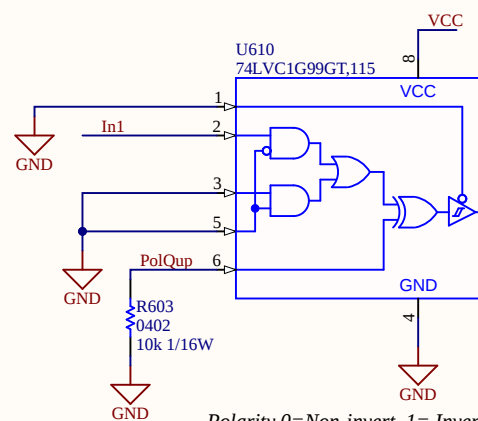
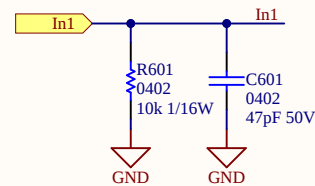
Buck Single Signal
Boost Single Signal
Dual Signal

Dual/Single PWM, Buck, and Boost Mode Selector



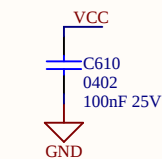
Full Bypass
DT Bypass
No Bypass

Bypass Mode Select

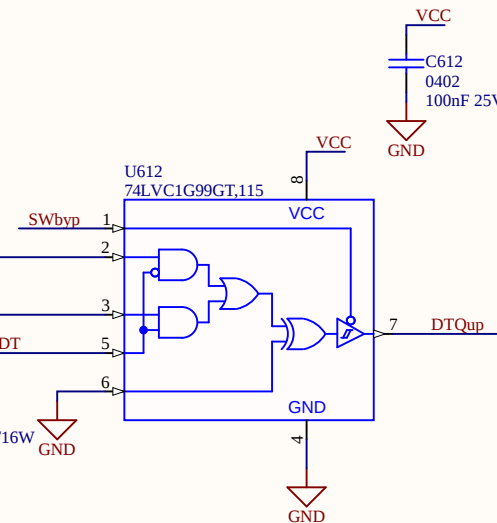


Polarity 0=Non-invert, 1= Invert

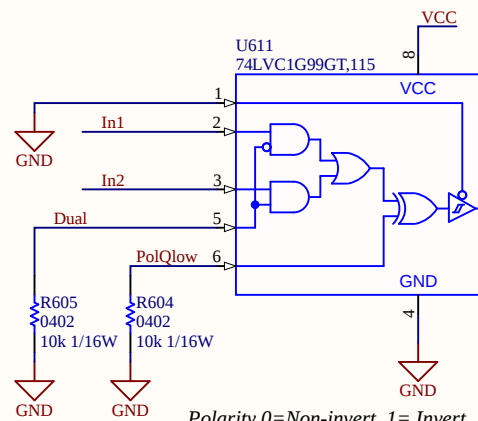
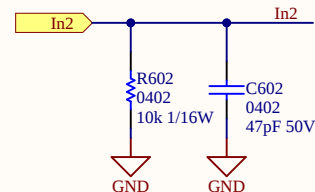
Signal Polarity and Input Buffers



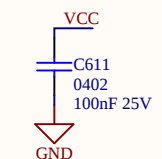
Deadtime Upper
Default = 10 ns



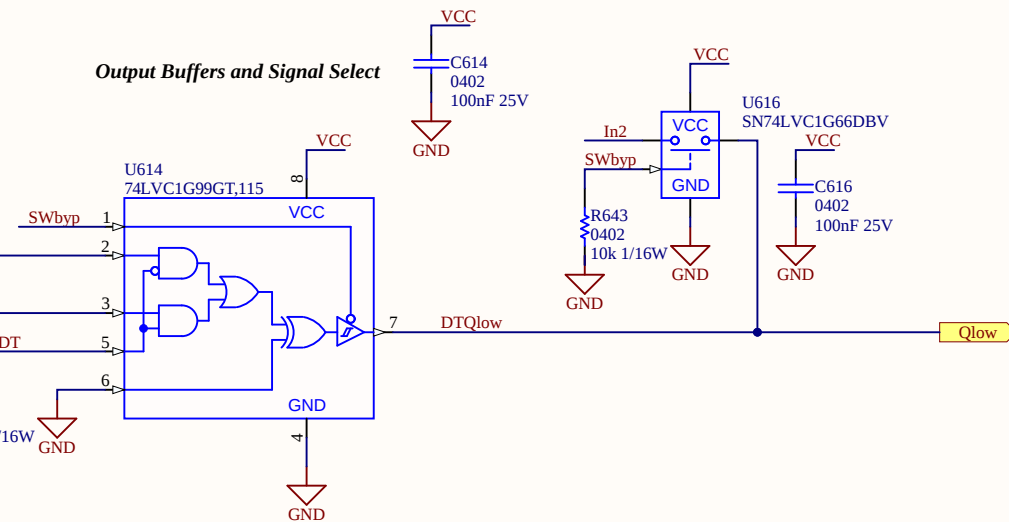
Output Buffers and Signal Select

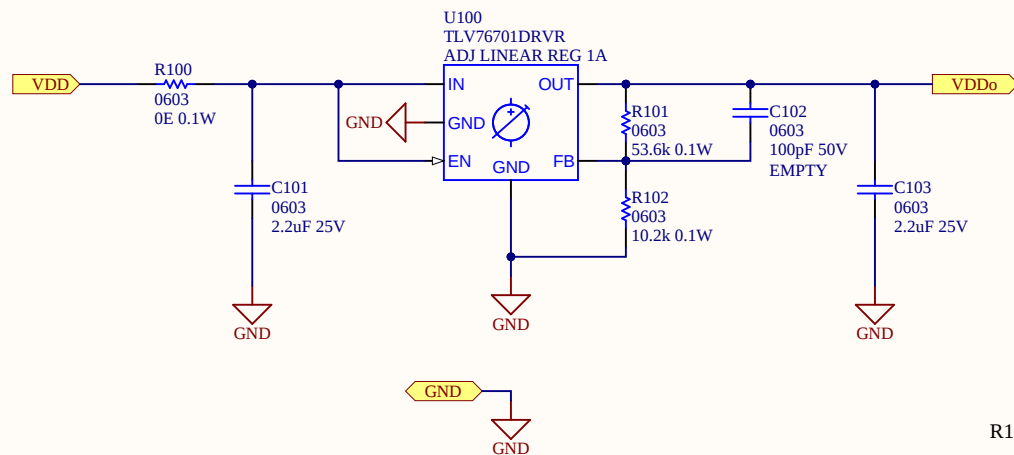


Polarity 0=Non-invert, 1= Invert



Deadtime Lower
Default = 10 ns





R101 R102 VDDo
53.6k 10.2k 5V
54.9k 10.2k 5.1V
56.2k 10.2k 5.2V
54.9k 9.76k 5.3V
56.2k 10.2k 5.4V
60k 10.2k 5.5V

Title: 16 V to 5 V, 1 A Linear Regulator

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Design #: AP1092

Revision 1.0

Date: 8/13/2026

File: AP1092_Rev1_0.SCHDOC

Sheet 4 of 5

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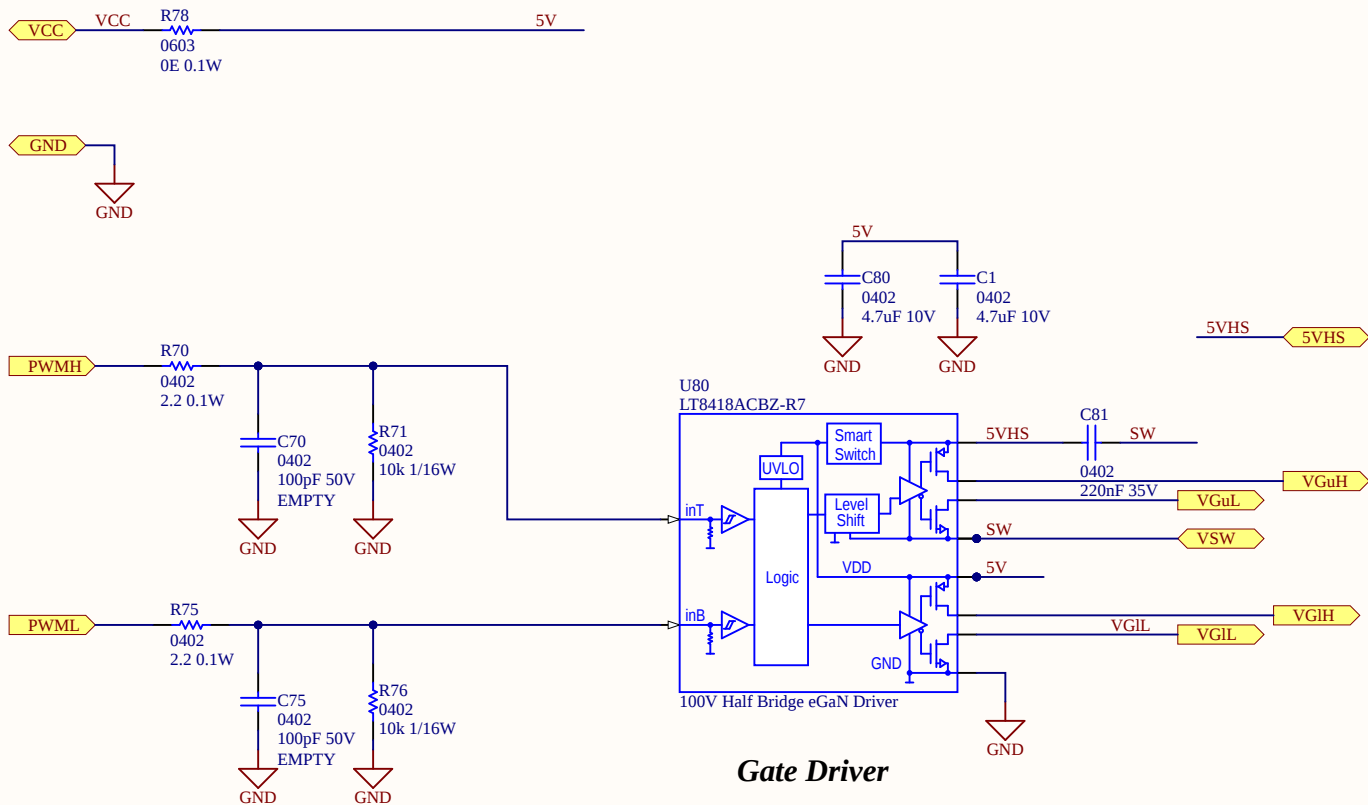
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Title: 100 V HB Gate Driver

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Design #: AP1093

Revision 1.0

Date: 8/13/2026

File: AP1093_Rev1_0.SCHDOC

Sheet 5 of 5

Efficient Power Conversion

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